REMARKS

The Office Action mailed November 17, 2003 has been received and reviewed. Figures 2, 8, and 10 are objected to as containing reference numerals not referred to in the patent specification. By this amendment, references to the reference numerals objected to have been added to the specification.

Claims 1-24 stand rejected. Claims 1, 4, 13 and 22-34 stand rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,996,690 to George et al. Claims 2 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over George in view of U.S. Patent No. 6,151,180 to Bang. Claims 5-10, 16-19 and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over George in view of U.S. Patent No. 4,189,765 to Kotalik et al. Claims 11, 12, and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over George in view of Kotalik and U.S. Patent No. 6,151,180 to Bang. Claims 3 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if written in independent form. Reconsideration of Claims 1-24 in view of the following remarks is respectfully requested.

REJECTION OF CLAIMS 1, 4, 13, AND 22-34 UNDER 35 U.S.C. 102(b) IN VIEW OF GEORGE

With respect to Claims 1, 22, and 24, Applicant respectfully asserts that the defense of anticipation is improper. In order for a cited reference to anticipate, every element of the claimed invention must be identically disclosed in a single cited reference; and those elements must be arranged or connected together in a single reference in the same way as specified in the patent claim. Applicant asserts that the cited reference does not recite the claimed structure.

Applicant respectfully asserts that George fails to disclose an error avoidance module as claimed by Applicant. The error avoidance module disclosed claimed by applicant is configured to

compare the capacity of a buffer to a count of bytes transferred into the buffer. George does not teach that the encoder 72 of George counts bytes and compares the number of bytes to the capacity of a buffer. The encoder 72 of George merely calculates a parity check bit for data. (Col. 7, lns. 48-52).

Furthermore, the method of Figure 6 of George performed by the encoder 72 is an algorithm for calculating a parity check bit which is based on a single byte (Col. 14, lns. 43-59; Figure 6, element 134 "Calculate Parity Digit Per Byte"). The parity check bit is not based on the capacity of a buffer 22, 24 or on the number of bytes transferred to the buffers 22, 24.

In addition, George fails to teach the forcing of any error condition as recited by Applicant. The end result of the method and apparatus of George is merely an encoded parity check bit.

With respect to Claim 13, Applicant respectfully asserts that George fails to teach providing a count of bytes stored in the buffer 22, 24. Applicant further asserts that George does not teach that the encoder 72 in anyway counts bytes stored in the buffers 22,24. George also fails to disclose forcing an error condition based on a count. The gating means 16,24 is in no way identified as forcing an error condition. George only teaches that the gating means serves only to halt the input of information into a buffer.

With respect to Claim 23, Applicant respectfully asserts that as discussed above, George fails to disclose an error avoidance module as claimed by applicant. Accordingly, George cannot teach an initialization module enabling an error avoidance module as claimed by Applicant.

REJECTION OF CLAIMS 2 AND 14 UNDER 35 U.S.C. 103(a) OVER GEORGE IN VIEW OF BANG

With respect to Claims 2 and 14, it is well established that in order to establish prima facie obviousness; (i) there must be some suggestion or motivation to modify the reference or to combine

reference teachings, (ii) there must be a reasonable expectation of success, and (iii) the prior art reference (or references when combined) must teach or suggest all the claimed limitations (MPEP 706.02(j)).

Applicant asserts that George does not include all of the limitations of Claims 1 and 13, as discussed hereinabove. Applicant further asserts that both Bang and George are inapposite. Applicant's invention monitors the input of bytes into a buffer. Bang, on the other hand, teaches a system for detecting corrupt data on a hard drive, (See Abstract), and George teaches a method for encoding error correcting data. (See Abstract). Accordingly, neither of these references is apposite here.

Furthermore, Bang teaches reporting the size of a defective block of data. (Column 4, lns. 39-59). On the other hand, Claims 1 and 13 count the size of bytes *transferred* into a buffer, not whether the bytes are defective.

Bang does not teach that the size of a defective block of data should be compared with the capacity of a buffer, as recited in Claims 2 and 13. To the contrary, the Error Correction Code of Bang relates only to whether "the capability of the servo controller 260 is sufficient to guarantee correction" (Col. 3, lns. 53-54) and has nothing to do with the capacity of a buffer.

There is also no teaching or suggestion to combine Bang and George. Bang relates to correcting hard disk errors and George relates to parity check bit encoding. Neither George nor Bang in any way suggest that comparing the size of a corrupt block of data to an ECC capability will in any way help or aid the calculation of a parity check bit.

REJECTION OF CLAIMS 5-10, 16-19, AND 20 UNDER 35 U.S.C. 103(a) OVER GEORGE IN VIEW OF KOTALIK

With respect to Claims 5-10 and 16-19, Applicant asserts that George does not teach all the elements of Claims 1 and 13 as discussed hereinabove. Furthermore, Kotalik is inapposite to George and to the claimed invention. Kotalik is a system for monitoring and controlling process variables. (See Abstract). Kotalik also does not relate in any way to monitoring the input of data into a buffer or to the calculation of parity check bits (George, Abstract).

Applicant further asserts that the upper and lower limits of Kotalik refer to a "control output signal." (Col. 3, lns. 28-36). Upper and lower limits recited by applicant relate to the bytes transferred into a buffer, not to control signals. Accordingly, Kotalik fails to teach a high or low capacity limit of a buffer as recited in claims of applicant.

Referring specifically to Claims 5 and 16, Kotalik fails to teach a content limiting interrupt. The upper and lower limits of Kotalik bound a continuous signal, they do not involve anything that may be deemed an "interrupt" as known in the art or as discussed by Applicant.

Referring specifically to Claim 9, Kotalik fails to teach a content-limiting interrupt triggering execution of an error avoidance module because Kotalik does not teach an error avoidance module as claimed by Applicant in Claims 1 and 13. Kotalik teaches no structure configured to be invoked by a driver to compare the capacity of a count of bytes transferred into a buffer with the capacity of the buffer as recited in Claims 1 and 13.

Referring specifically to Claim 10, neither Kotalik nor George teach any structure detecting read and write operations.

Referring specifically to Claim 20, neither Kotalik nor George teach that a count is initialized when the control signal reaches a high or low.

Finally, there is no teaching or suggestion to combine Kotalik and George. Kotalik does not involve the calculation of a parity check bit and George does not involve the processing of control signals. George in no way suggests that the values of a parity check bit would need to be bound by an upper or lower limit. Furthermore, George does not seek to avoid errors but rather the calculation of a prity check bit to detect and correct errors. (Col. 1, lns. 37-43.)

REJECTION OF CLAIMS 11, 12, AND 21 UNDER 35 U.S.C. 103(a) OVER GEORGE IN VIEW OF KOTALIK AND BANG

First, with respect to Claims 11, 12, and 21, Applicant asserts that all elements of claims 1, 13, 9 and 20 are not found in George, Kotalik, and Bang, whether separately or in combination, as discussed hereinabove. Accordingly, a prima facie case of obviousness has not been established.

Second, George, Bang, and Kotalik are inapposite art as discussed hereinabve. Neither Bang Kotalik, nor George bears any relation to the detection of errors in buffers. Accordingly, it would not have been obvious to combine them to arrive at the claimed invention. Moreover, combining them does not result in the invention.

Third, there is no teaching or suggestion to combine the upper and lower limits of Kotalik with the FIFO buffer of Bang. Kotalik does not in any way relate to buffers or error avoidance. Accordingly, Kotalik cannot possibly teach a combination of its teachings with those of Bang. Meanwhile, Bank does not contain any suggestion that it would serve in the system of Kotalik.

Referring specifically to Claim 11, the R/W AGC & Filter 212 of Bang only detect read signals (Col. 3, lns. 40-49) and Bang makes no suggestion that it should operate on write signals. Furthermore, the R/W AGC & Filter 212 is not an error avoidance module as recited claimed by applicant. Element 212 does not compare the capacity of a buffer to a count of bytes transferred into a buffer as does the error avoidance module claimed by Applicant.

In view of the foregoing remarks, Applicant believes the claims to be in condition for allowance. Reconsideration of Claims 1-24 in view of the above remarks is therefore respectfully requested. In the event the examiner finds any impediment to the allowance of the claims, Applicant respectfully requests that the examiner call the undersigned.

DATED this 10th day of February, 2004.

Respectfully submitted,

A. John Pate
Registration No. 36,234
Attorney for Applicant

Date: February 10, 2004

PATE PIERCE & BAIRD
550 Parkside Tower
215 South State Street
Salt Lake City, Utah 84111
Telephone: (801) 530-0330
Facsimile: (801) 530-5955

Z:\ALL CLIENTS\2456 Adams\2456-2-9\2456-2-9 PAT-FIL-Amendment A 040210.wpd